



SMC-02-1308

December 15, 2003

To: Commissioner for Patents  
P.O.Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
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Subject: | Serial No. 10/672,395 09/26/03 |  
C.H. Yu et al.  
METHOD OF SELECTIVELY MAKING COPPER  
USING PLATING TECHNOLOGY  
| \_\_\_\_\_ |

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
mail in an envelope addressed to: Commissioner for Patents,  
P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 12/19/03

U.S. Patent 6,420,258 to Chen et al., "Selective Growth of Copper for Advanced Metallization," describes a recent advance in copper deposition which involves a selective growth of copper by an electrochemical method on a conformal seed layer in a trench.

U.S. Patent 6,153,935 to Edelstein et al., "Dual Etch Stop/Diffusion Barrier for Damascene Interconnects," discloses a diffusion barrier cap selectively deposited on a metal interconnect which provides corrosion protection and improved electromigration resistance.

U.S. Patent 6,441,492 to Cunningham, "Diffusion Barriers for Copper Interconnect Systems," discusses a barrier layer which is rhenium, rhodium, or ruthenium formed on a copper interconnect and affords high resistance to Cu diffusion.

U.S. Patent 6,004,188 to Roy, "Method for Forming Copper Damascene Structures by Using a Dual CMP Barrier Layer," discloses an improved and new method for forming dual damascene CMP of copper lines and interconnects(studs) using a dual CMP barrier layer.

U.S. Patent 6,417,095 to Chen, "Method for Fabricating a Dual Damascene Structure," discusses a sacrificial layer used which eliminates the need for a CMP step.

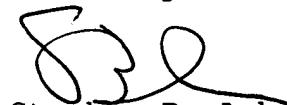
TSMC-02-1308

U.S. Patent 6,528,426 to Olsen et al., "Integrated Circuit Interconnect and Method," discusses a SiC CMP stop layer utilized to protect an underlying mechanically weak dielectric layer such as porous SiO<sub>2</sub>.

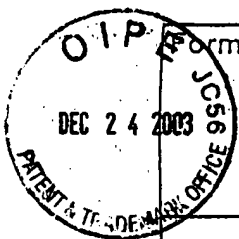
U.S. Patent 6,509,267 to Woo et al., "Method of Forming Low Resistance Barrier on Low K Interconnect with Electrolessly Plated Copper Seed Layer," discusses conformal nitride and Ta barrier layers being formed on the sidewalls of a dielectric layer to prevent Cu from being sputtered onto the dielectric layer during a via etch.

U.S. Patent 6,482,741 to Ueno, "Copper Wiring Structure Comprising a Copper Material Buried in a Hollow of an Insulating Film and a Carbon Layer Between the Hollow and the Copper Material in Semiconductor Device and Method Fabricating the Same," discusses a carbon electroconductive layer formed on the sidewalls and bottom of an opening in an amorphous C and F containing dielectric layer by a plasma treatment.

Sincerely,



Stephen B. Ackerman,  
Reg. No. 37761



Form PTO-1449

INFORMATION DISCLOSURE CITATION  
IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Sequence)

TSMC-02-1308

Application Number

10/672,395

Applicant

C.H. Yu et al.

Filing Date

09/26/03

Group Art Unit

## U. S. PATENT DOCUMENTS

| EXAMINER<br>INITIAL | DOCUMENT NUMBER | DATE     | NAME             | CLASS | SUBCLASS | PLUNG DATE<br>IF APPROPRIATE |
|---------------------|-----------------|----------|------------------|-------|----------|------------------------------|
|                     | 6420258         | 7/16/02  | Chen et al.      | 438   | 622      | 11/12/99                     |
|                     | 6153935         | 11/28/00 | Edelstein et al. | 257   | 773      | 9/30/99                      |
|                     | 6004188         | 12/21/99 | Rey              | 451   | 41       | 9/10/98                      |
|                     | 6417095         | 7/9/02   | Chen             | 438   | 633      | 6/11/01                      |
|                     | 6528426         | 3/4/03   | Olsen et al.     | 438   | 689      | 10/15/99                     |
|                     | 6509267         | 1/21/03  | Woo et al.       | 438   | 687      | 6/20/01                      |
|                     | 6482741         | 11/19/02 | Keno             | 438   | 687      | 8/20/99                      |
|                     | 6441492         | 8/27/02  | Cunningham       | 257   | 762      | 9/28/00                      |
|                     |                 |          |                  |       |          |                              |
|                     |                 |          |                  |       |          |                              |
|                     |                 |          |                  |       |          |                              |

## FOREIGN PATENT DOCUMENTS

|  | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation |    |
|--|-----------------|------|---------|-------|----------|-------------|----|
|  |                 |      |         |       |          | YES         | NO |
|  |                 |      |         |       |          |             |    |
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|  |                 |      |         |       |          |             |    |
|  |                 |      |         |       |          |             |    |
|  |                 |      |         |       |          |             |    |

## OTHER DOCUMENTS (Including Author, Title, Date, Portion of Pages, Etc.)

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EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.